ML2002 Series Static/Half Duty LCD COG Driver

❖ *Application*

- *General Purpose Clock*
- *High quality instrument*
- *Telephone, mobile phone*
- *Automotive*
- *Handheld Device like PDA, MP3, or PMP*

❖ *Features*

- A Gold Bump Chip which can reduce pin count and area.
- Simplest design with no charge pump to supply high voltage to LCD
- Only 5 pin is needed which can reduce space.
- Low operating current
- Can disable internal clock to reduce current.
- Wide Logic & LCD power supply: 2.5V to 6.0V
- No need to add external voltage regulator
- Static or 1/2 Duty driving with 1/2 Bias
- Number of segments: (Static) 48, (1/2 Duty) 96
- Cascading structure to increase the number of driving segments, it's more flexible for different application.
- Build-in LCD voltage driver, crystal oscillator, internal RC oscillator and display control circuit.
- Offer best contrast and widest viewing angle of TN LCD technology especially in static mode.
- No temperature compensation is needed for Topr = -40°C to 80°C.

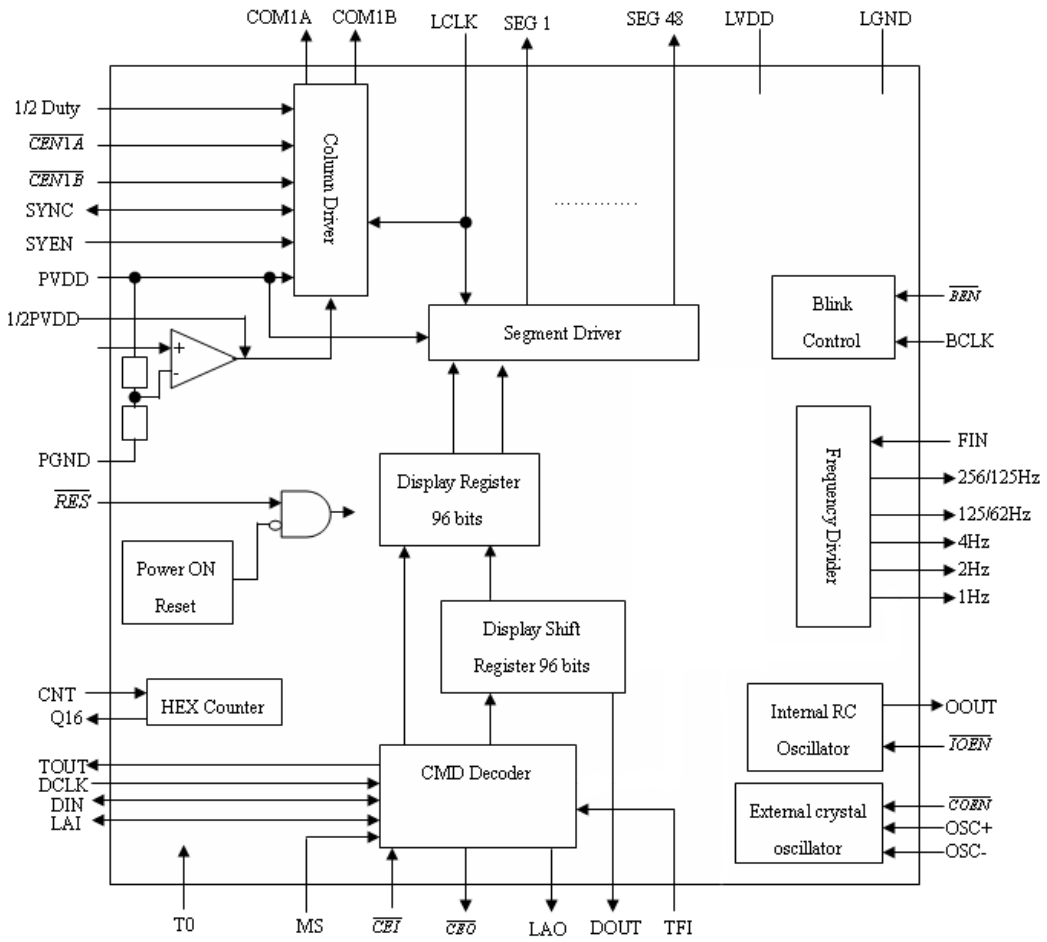
❖ *General Description*

ML2002 (COG) LCD driver can be cascaded to increase the number of segments drive, with Static driving it can form a single piece of 48 (1 ICs) or 96 (2 ICs cascaded) segments driver. With 1/2 Duty, the number of segment drive would be doubled. It targets at custom TN LCD COG Module product which requires the best quality of TN LCD technology and small to medium number of segment display. ML2002 series driver offers the best contrast, the widest viewing angle, the widest range of operating voltage and temperature when compared to the high duty cycle driver. EMI and Noise protection circuit has been added which tailor made for COG application.

❖ *Ordering Information*

Part Number	Description	Package Form
ML2002-1U	One ML2002 LCD driver	Gold Bump Die
ML2002-2U	Two ML2002 LCD driver	Gold Bump Die

❖ *Block Diagram*



❖ *Absolute Maximum Ratings*

Parameter	Symbol	Condition	MIN	MAX	Unit
Supply voltage	V_{DD}		-0.5	+6.0	V
Supply Current	I_{DD}	V_{DD} = 3V, no Load	-50	+50	mA
Input Voltage	V_{IN}		GND-0.3	V_{DD} +0.3	V
Output Voltage	V_{OUT}		GND-0.3	V_{DD} +0.3	V
DC input Current	I_{IN}		-10	+10	mA
DC output Current	I_{OUT}		-10	+10	mA
Storage temperature	T_{stg}		-65	+150	°C
Total power dissipation	P_{tot}		-	400	mW

❖ *DC Characteristic*

V_{DD} = 3.0V; T_{amb} = 25°C ; unless otherwise specified

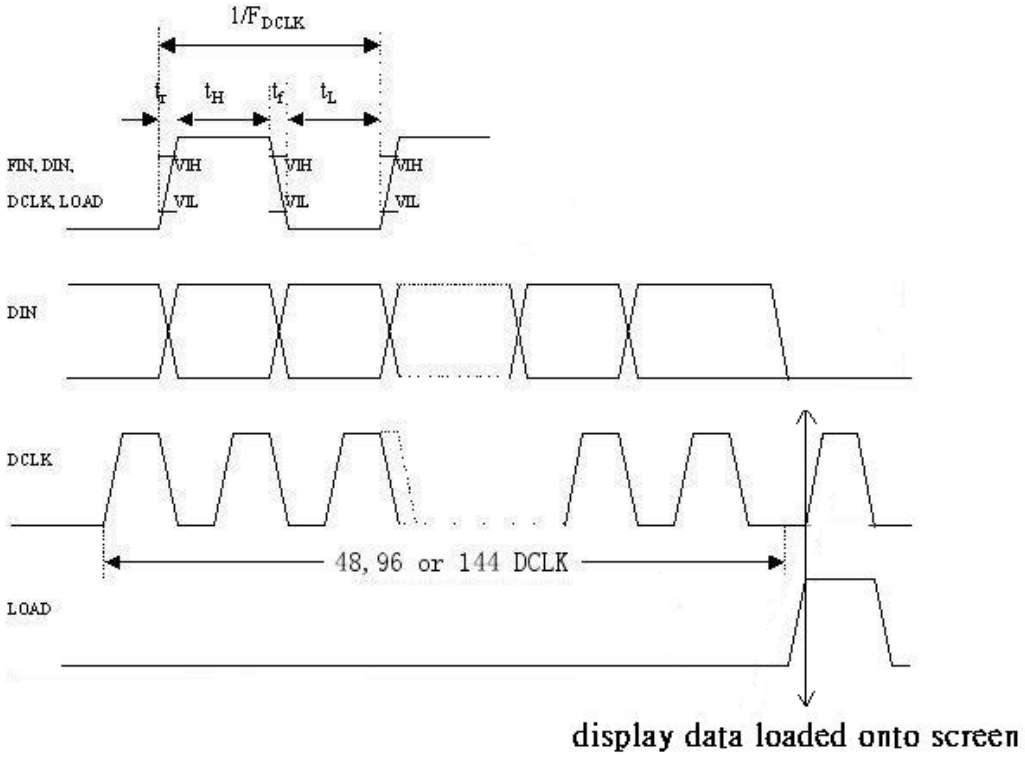
Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supplies						
Supply voltage	V_{DD}		2.5	-	6.0	V
Supply Current	I_{DD}	Disable Oscillator and 1/2 PVDD opamp	-	0.1	0.5	uA
Supply Current	I_{DD}	Enable Oscillator	-	25	60	uA
Supply Current	I_{DD}	Enable Oscillator and Internal 1/2 PVDD opamp	-	80	100	uA
Logic						
LOW-level input voltage	V_{IL}		GND	-	0.3*V_{DD}	V
HIGH-level input voltage	V_{IH}		0.7*V_{DD}	-	V_{DD}	V
LOW-level output current	I_{OL}	V_{OL} = 1.0V	1	-	-	mA
HIGH-level output current	I_{OH}	V_{OH} = 2.0V	-1	-	-	mA
LCD outputs						
Output resistance at pads S1 to S40	R_{SEG}		-	85	150	ohm
Output resistance at pads COM1A and COM1B	R_{COM}		-	45	100	ohm

❖ *AC Characteristic*

V_{DD} =3.0V; T_{amb} = 25°C; unless otherwise specified

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Oscillator frequency at pad OOUT	f_{oout}		21	32	48	kHz
FIN, LOAD, DIN, DCLK High time	t_H		0.4	-	-	us
FIN, LOAD, DIN, DCLK Low time	t_L		0.4	-	-	us
FIN, LOAD, DIN, DCLK Rise time	t_r		-	-	10	us
FIN, LOAD, DIN, DCLK Fall time	t_f		-	-	10	us
DCLK Frequency	F_{DCLK}		1	-	250	kHz

❖ *Timing Diagram for slave mode display*



With MS connected to GND, it represents it is in slave mode, it will treat all the DIN data as display data and will be sent to ML2002's display shift register directly through DIN and DCLK.
To Load display data onto the screen, LAI need to be high, then a rising edge of DCLK would load the display, the LAI need to keep low again.

❖ *Functional Description*

There are 48 Segments in Static Mode, and 96 Segments in 1/2 Duty Mode with 1/2 Bias. The display data should be input in reverse order, for static it's starting from SEG48, SEG47… SEG2 to SEG1, for 1/2 duty it's starting from SEG48-COMB, SEG48-COMA … SEG1-COMB to SEG1-COMA for proper display of data. When updating the display, it will require inputting 48 Segments in Static Mode and 96 Segments in 1/2 Duty Mode.

i) Internal Power on reset

At power on the ML2002 will reset the internal display Data RAM as cleared.

ii) Oscillator

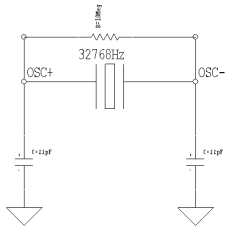
The LCD driving signal of ML2002 is clocked either by the built-in oscillator, crystal oscillator or from an external clock.

a) Internal clock

When the internal oscillator is used, BIOEN should be connected to GND and the OOUT should be connected to FIN. The internal oscillator will oscillate at 32 kHz and the frequency is independent in the range of $2.5V \leq V_{DD} \leq 6.0V$. Then connect OOUT to FIN.

b) Crystal clock

When using the crystal oscillator, BCOEN is connected to GND, then connect the crystal to OSC+, and OSC-. Then connect OSC- to FIN. The OSC+ and OSC- should connect as:



c) External clock

When using an external clock, BCOEN & BIOEN is connected to VDD then connects the external clock to FIN (32 KHz) or LCLK (125Hz)

iii) Timing

ML2002 have several frequencies of clock signal for the users to choose for the LCD display clock (ie. LCLK) and the blink clock (ie.BCLK). They include the following clock signals:

Frequency of Clock Signal at FIN = 32 kHz	Actual Divider of FIN	Target Input Pin
256/128 Hz	1/256(1/2 Duty) or 1/128(Static)	LCLK
128/64 Hz	1/128(1/2 Duty) or 1/64(Static)	
4 Hz	1/8192	BCLK
2 Hz	1/16384	
1 Hz	1/32768	

iv) Segment outputs

ML2002 has 48 segment outputs which should be connected directly to the LCD. If less than 48 segments, the unused segments should be left open circuit.

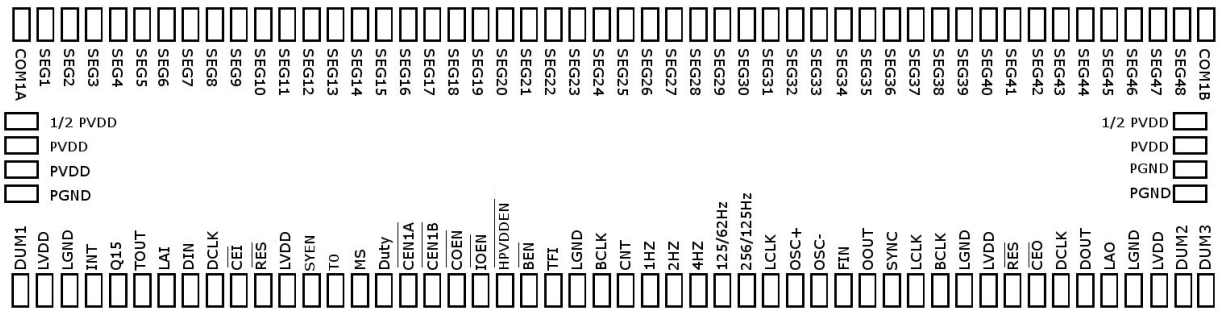
v) Common outputs

ML2002 consists of 2 common signals (ie. COM1A & COM1B). The common outputs should be left open-circuit if the outputs are unused. Users can disable the COM1A and COM1B by connecting the $\overline{CEN1A}$ and $\overline{CEN1B}$ to VDD respectively. The common outputs will change to GND after disabling it.

vi) Blink

ML2002 has a blink function that users shall connect $\overline{BEN}$ to GND and input the blink clock (ie. BCLK) either by connecting ML2002 output clock signal from Frequency Divider or an external clock signal. Users shall disable blink function by connecting $\overline{BEN}$ to VDD.

❖ *Pad Configuration*



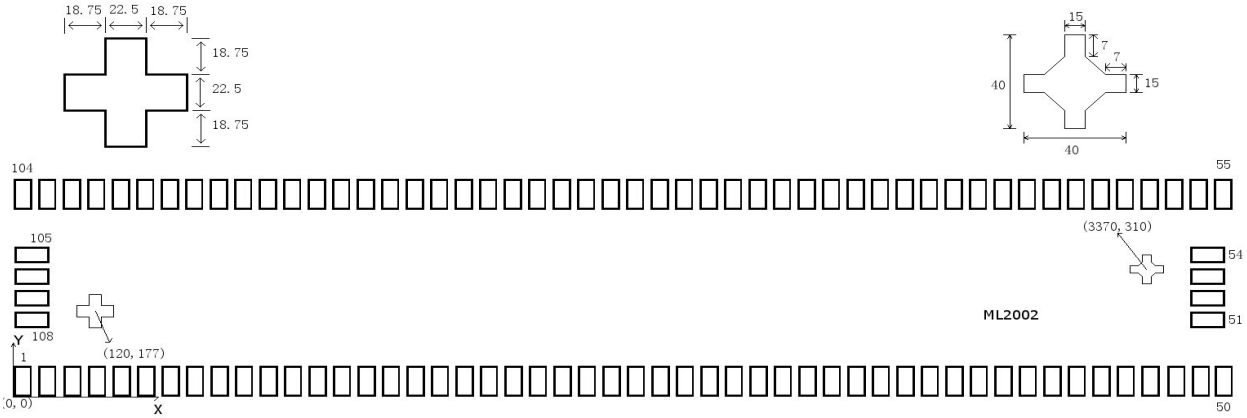
Chip Size :

Part Number	Description	Chip Size
ML2002-1U	One ML2002 LCD driver	3660 x 660
ML2002-2U	Two ML2002 LCD driver	7320 x 660

Chip Thickness : 700 um $\pm$ 25 um
Gold Bump Pad Size : 32 um x 72 um
Gold Bump Height : 18 um $\pm$ 2 um

Note :
The die faces up in the diagram

* Pad Orientation and Alignment Mark:



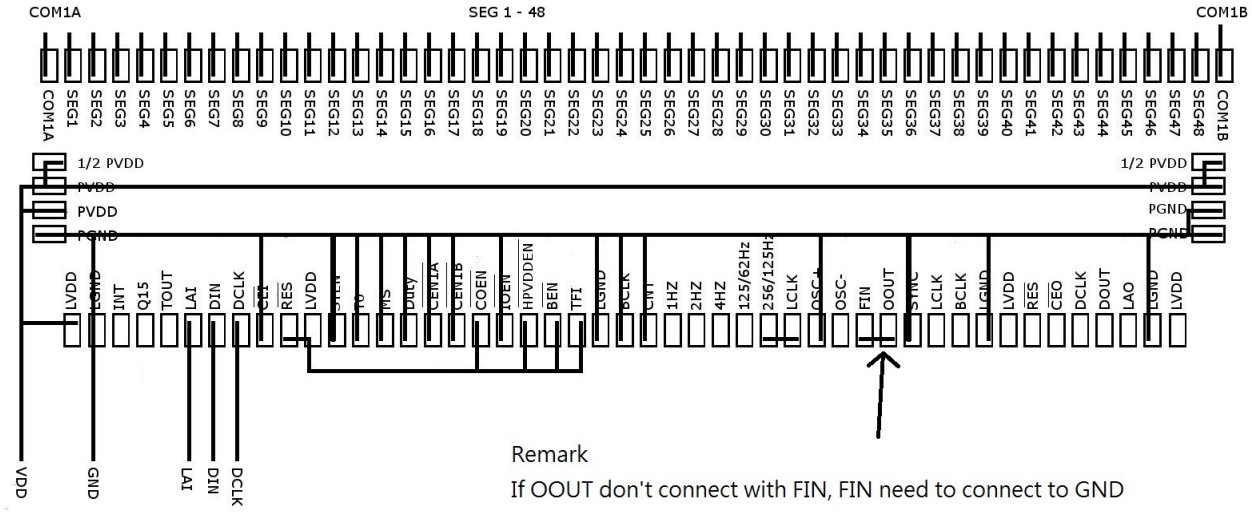
Pad	Pad Name	X	Y	Pad	Pad Name	X	Y	Pad	Pad Name	X	Y
1	DUM1	0	0	51	PGND	3390	110	101	SEG3	210	390
2	LVDD	70	0	52	PGND	3390	180	102	SEG2	140	390
3	LGND	140	0	53	PVDD	3390	250	103	SEG1	70	390
4	INT	210	0	54	1/2PVDD	3390	320	104	COM1A	0	390
5	Q15	280	0	55	COM1B	3430	390	105	1/2PVDD	0	320
6	TOUT	350	0	56	SEG48	3360	390	106	PVDD	0	250
7	LAI	420	0	57	SEG47	3290	390	107	PVDD	0	180
8	DIN	490	0	58	SEG46	3220	390	108	PGND	0	110
9	DCLK	560	0	59	SEG45	3150	390				
10	CEI	630	0	60	SEG44	3080	390				
11	RES	700	0	61	SEG43	3010	390				
12	LVDD	770	0	62	SEG42	2940	390				
13	SYEN	840	0	63	SEG41	2870	390				
14	TO	910	0	64	SEG40	2800	390				
15	MS	980	0	65	SEG39	2730	390				
16	DUTY	1050	0	66	SEG38	2660	390				
17	CEN1A	1120	0	67	SEG37	2590	390				
18	CEN1B	1190	0	68	SEG36	2520	390				
19	COEN	1260	0	69	SEG35	2450	390				
20	IOEN	1330	0	70	SEG34	2380	390				
21	HPVDDEN	1400	0	71	SEG33	2310	390				
22	BEN	1470	0	72	SEG32	2240	390				
23	TFI	1540	0	73	SEG31	2170	390				
24	LGND	1610	0	74	SEG30	2100	390				
25	BCLK	1680	0	75	SEG29	2030	390				
26	CNT	1750	0	76	SEG28	1960	390				
27	1HZ	1820	0	77	SEG27	1890	390				
28	2HZ	1890	0	78	SEG26	1820	390				
29	4HZ	1960	0	79	SEG25	1750	390				
30	125/62HZ	2030	0	80	SEG24	1680	390				
31	256/125HZ	2100	0	81	SEG23	1610	390				
32	LCLK	2170	0	82	SEG22	1540	390				
33	OSC+	2240	0	83	SEG21	1470	390				
34	OSC-	2310	0	84	SEG20	1400	390				
35	FIN	2380	0	85	SEG19	1330	390				
36	QOUT	2450	0	86	SEG18	1260	390				
37	SYNC	2520	0	87	SEG17	1190	390				
38	LCLK	2590	0	88	SEG16	1120	390				
39	BCLK	2660	0	89	SEG15	1050	390				
40	LGND	2730	0	90	SEG14	980	390				
41	LVDD	2800	0	91	SEG13	910	390				
42	RES	2870	0	92	SEG12	840	390				
43	CEO	2940	0	93	SEG11	770	390				
44	DCLK	3010	0	94	SEG10	700	390				
45	DOUT	3080	0	95	SEG9	630	390				
46	LAO	3150	0	96	SEG8	560	390				
47	LGND	3220	0	97	SEG7	490	390				
48	LVDD	3290	0	98	SEG6	420	390				
49	DUM2	3360	0	99	SEG5	350	390				
50	DUM3	3430	0	100	SEG4	280	390				

Note: Pad 1, 49 and 50 are DUM Pads which must be open.

❖ *Application Circuit*

ML2002 Single Chip Connection

1. ML2002 1U Static Slave Mode



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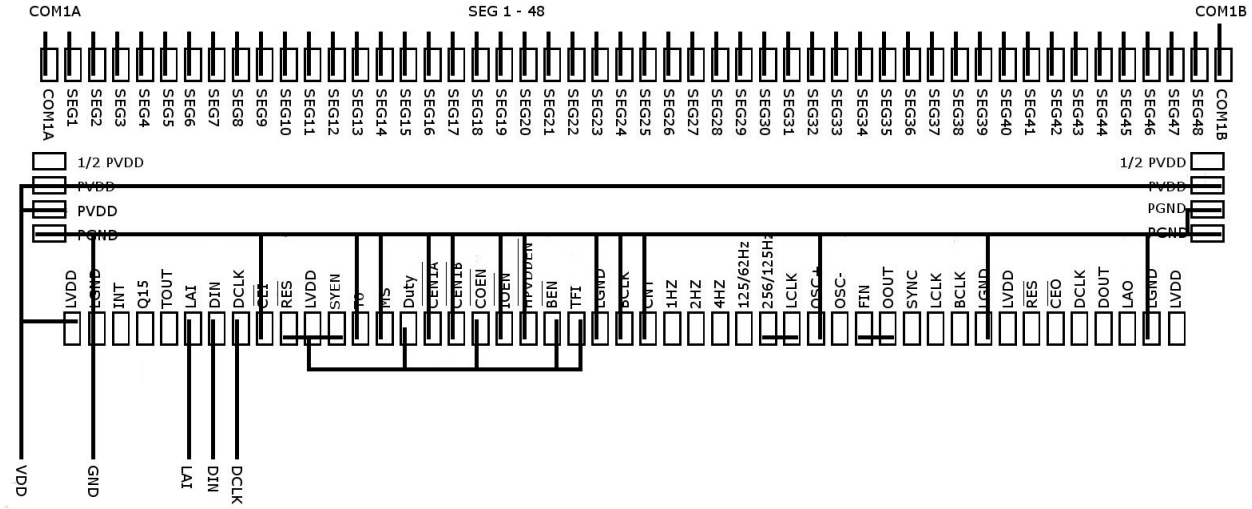
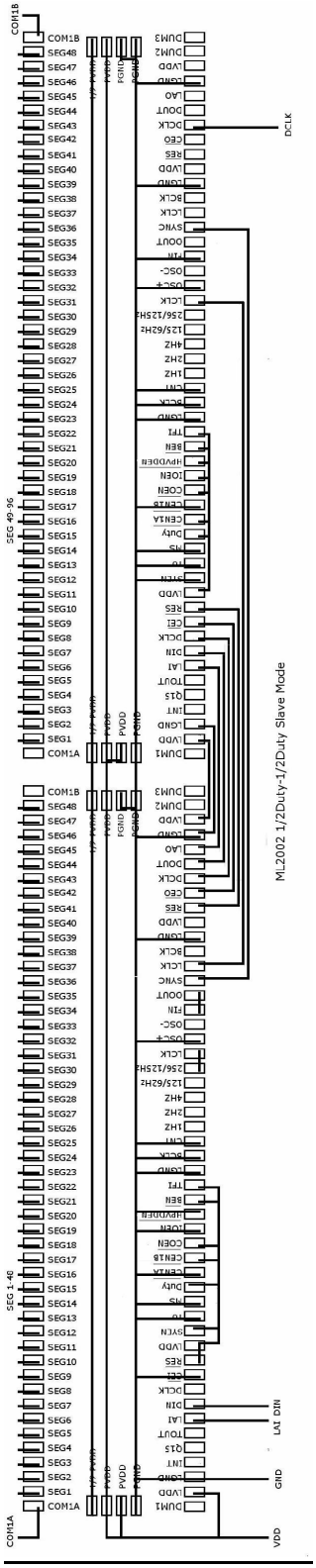
2. ML2002 1U 1/2 Duty Slave Mode



ML2002 Cascode Structure Connection

1. ML2002 2U 1/2Duty-1/2Duty Slave-Slave Mode



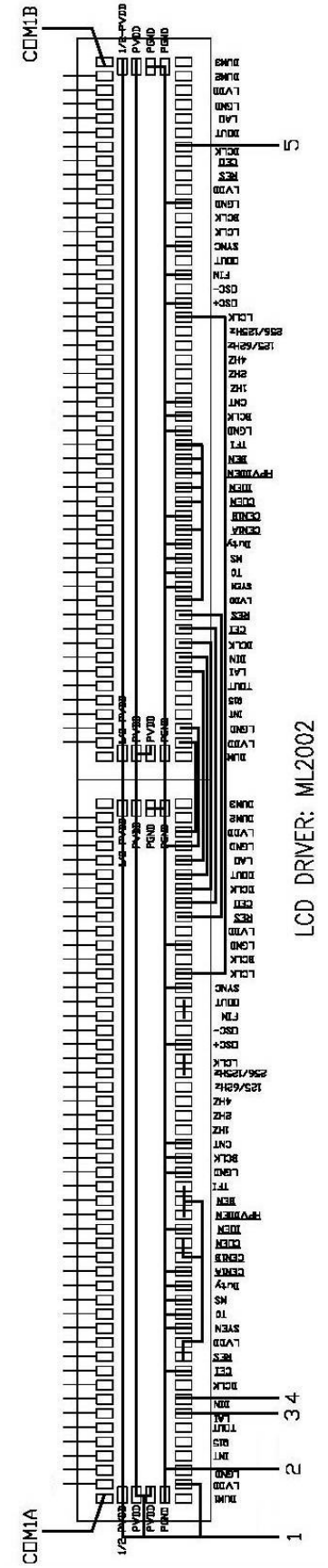
Working Glass Size:

Length = 64.80 V.A

Width = 35.40 V.A

(Unit: mm)

2. ML2002 2U Static Slave-Slave Mode



Working Glass Size:

Length = 76.00 V.A

Width = 59.95 V.A

(Unit: mm)

❖ *Pin Description*

SYMBOL	PAD	DESCRIPTION
$\overline{BRES}$	I	External reset input (active LOW)
LGND	-	Logic Ground
INT	I	Alarm interrupt output
LVDD	-	Logic Supply voltage
MS	I	Input "0", for slave mode
DIN	I	Data line input
DCLK	I	Data clock input
LAI	I/O	It is an input pin which LOAD the display onto the LCD screen during rising edge.
LAO	O	Send out LOAD signal to the cascade slave ML2002 for displaying data onto LCD screen.
$\overline{CEI}$	I	Enable Chip for receive data/command in the DIN pin
$\overline{CEO}$	O	Send out chip enable signal to the following cascade slave IC
DOUT	O	Data output from the display data RAM
CNT	I	Input clock, count number of rising edge clock
Q15	O	Output High on the 16th clock from CNT
FIN	I	32768Hz Oscillator input
4,2,1Hz	O	4, 2, 1Hz clock output
256/125 Hz	O	125Hz clock output for static/ 250 clock output for 1/2 duty
125/62 Hz	O	62Hz clock output for static/125 clock output for 1/2 duty
LCLK	I	LCD Clock signal frequency
SEG1 .. SEG48	O	Segment output
COM1A / B	O	Common output
PVDD	-	Power VDD supply
1/2 PVDD	I	1/2 PVDD LCD driving voltage
1/2 Duty	I	"1" – Halfduty, "0" – Static
$\overline{CEN1A}$, $\overline{CEN1B}$	I	Common Enable. "0" – Enable, "1" – Disable
T0	I	Test mode. "0" – Normal mode, "1" – Testing Mode
OOUT	O	32K internal clock output
$\overline{COEN}$	I	Crystal oscillator enable. "0" – Enable, "1" – Disable
$\overline{IOEN}$	I	32K internal clock enable. "0" – Enable, "1" – Disable
$\overline{HPVDDEN}$	I	1/2 PVDD enable. "0" – Enable, "1" – Disable
$\overline{BEN}$	I	Blink control circuit enable "0" – Enable, "1" – Disable
BCLK	I	Blink clock input
OSC+ / -	I	Crystal oscillator input
SYNC	I/O	To synchronize COMMON signal to the following cascade IC
TFI	I	Master mode 2/4 pin interface, "1" - 2pin , "0" - 4pin
SYEN	I	SYNC enable. SYEN is "1" – SYNC output, "0" – SYNC will be high impredence.
TOUT	O	When select 4pin interface, it would output timer data.
DUM1,2,3	-	Dummy Pad, Left it open only

Note : 1. In cascade format of ML2002(ie. ML2002-2U and –3U), one pin is the input of current ML2002 and the other is for the connection with the corresponding input pin of next ML2002.

2. Condition : FIN = 32 KHz Clock.

❖ *Application Note*

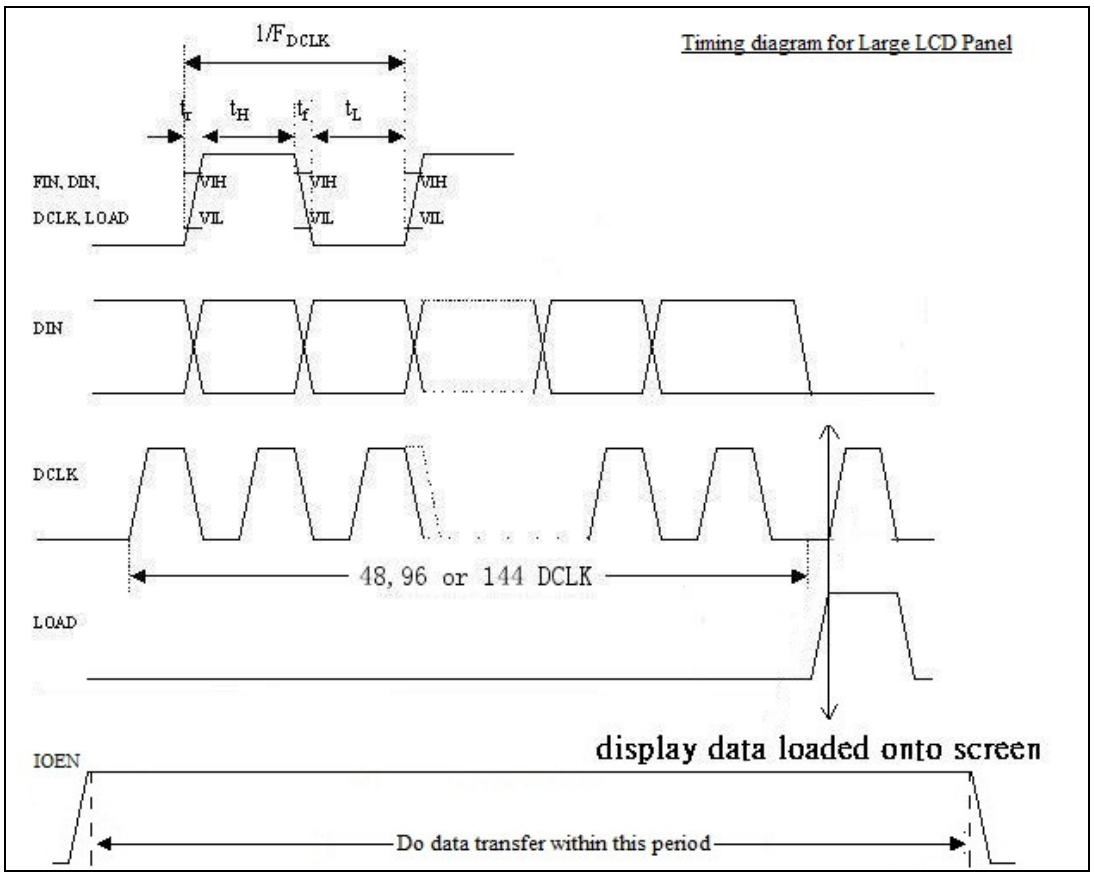
1. To ensure the good flip-chip assembly quality, we suggest flip-chip bonding house add a "CHECK" pin for each COG module as shown on the section of "Application Example". Pin "LOAD" and Pin "CHECK" shall be connected together if the flip-chip assembly is in good condition. The measured resistance between Pin "LOAD" and Pin "CHECK" shall not more than 5 kohm.

2. The resistance of ITO glass shall between 15 ohm/□ to 25 ohm/□.

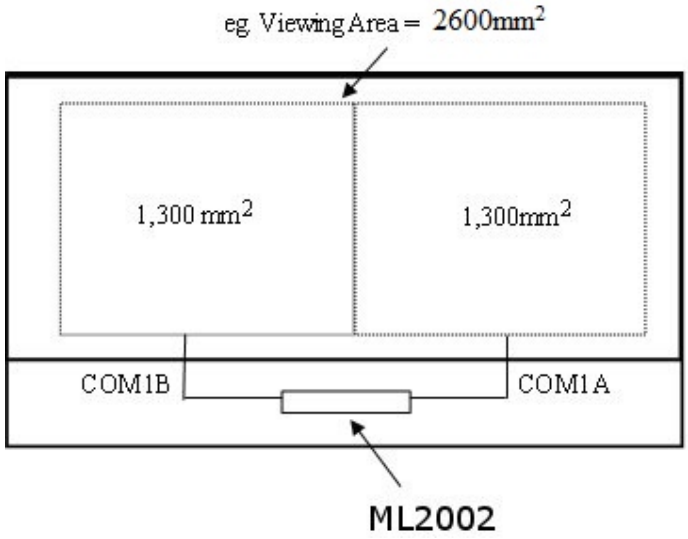
3. Each Common (ie. COM1A and COM1B) shall not cover more than 2,000 mm^2 area. In case the Viewing area of LCD has to be more than 2,000 mm^2, IOEN pin has to be connected to outside. At the time where data is transferring into the IC, internal oscillator has to be disabled through IOEN pin to prevent abnormal behavior. When data transfer finishes, internal oscillator has to be enabled again.

   Suggested programming steps:

1	Disable internal oscillator through IOEN pin
2	Delay (Necessary for fast MCU)
3	Transfer data through DIN, DCLK, LOAD
4	Delay (Necessary for fast MCU)
5	Enable internal oscillator through IOEN pin



Example :



Note : COM1A and COM1B shall cover half of the Viewing Area (ie. Area = 1,300mm^2)
Each Common shall not connect to each other.

❖ *Revision History*

Version 0.1 – Preliminary
Version 0.2 – Change Alignment mark co-ordinate on page 7
Add application note on page 12
Modify Application Circuit on page 8 – 10.
Updating Feature list on page 1
Updating Functional Description on page 4
Version 0.3 – Change Supply current condition with disable oscillator and internal PVDD opamp
Remove Real time clock in block diagram
Version 0.4 – Add Application Note when glass size area is larger than 2000mm^2 for each COM
Version 0.5 – Add Timing diagram for using large LCD panel
Version 0.6 – Add remark on page 8, for FIN connect to GND if OOUT don't connect with FIN.